VI523R

Product Description

VI523R is a highly-integrated, low-power monolithic ASK/OOK RF receiver chip. All high-frequency signal receiving functions are integrated on-chip to achieve the most reliable receiving performance with minimum peripheral components and lowest cost. It is a true single-chip receiving device featuring “wireless high-frequency modulated signal input and digital demodulated signal output”.

VI523R comes in an SOP8 package. Its normal operating voltage ranges from 2.2 V to 5.0 V, typical operating current is 5.0-5.2 mA, start-up time is 4 ms (with 470 nF external capacitor on CTH pin), and its maximum receiving sensitivity reaches -112 dBm. It is well-suited for various low-power-demand equipment. All RF and IF tuning is completed on-chip, eliminating manual adjustment during development and production, which reduces costs and accelerates time-to-market.

Features

Operating frequency band	300 - 490 MHz
Data rate range	1 - 5 kbps
Sensitivity	-112 dBm（3 kbps）, 0.1％ BER
Receiver bandwidth	500 kHz @ 433.92 MHz
	400 kHz @ 315 MHz
Start up time	4ms（CTH=470NF）
Image rejection ratio	30 dB
Maximum input signal	-20 dBm
Supply voltage	2.2 - 5.5 V
ow power consumption	5.0mA @ 315 MHz
	5.2mA @ 433.92 MHz



Applications

Remote control access control systems
Tire pressure monitoring devices
Remote control fans and lighting switches
Wireless sensor data transmission
Infrared receiver replacement
Toy remote controls

目录

Product Description 1
Features 1
Applications 1
1、Pin Definition and Description 1
1.1 Pin Diagram 1
1.2 Pin Description 1
2、 Absolute Maximum Ratings 2
3、 Recommended Operating Conditions 2
4、 Electrical Characteristics 3
5、Functional Description 4
5.1 Block Diagram 4
5.2 Crystal Frequency and RF Operating Frequency 4
5.3 Receiver Intermediate- Frequency Bandwidth 5
5.4 Notes on CTH Component Selection 5
6、Typical Application Circuit 6
6.1 Typical Schematic 6
6.2 Typical Circuit BOM 6
7、Package 7

1、Pin Definition and Description

1.1 Pin Diagram

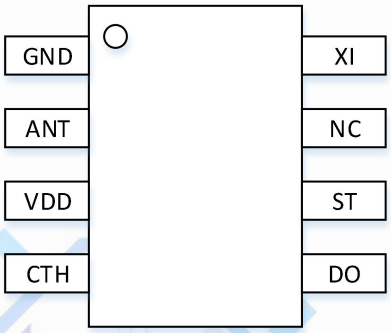

Figure 1 VI523R Pin Diagram

1.2 Pin Description

Table 1 VI523R Pin Descriptions

Pin No.	Pin Name	I/O	Pin Function Description
1	GND	P	Ground
2	ANT	I	RF signal input pin
3	VDD	P	Power- supply input, 2.1- 5.5V
4	CTH	I/O	For received- data filtering; connect external filter capacitor
5	DOUT	O	Received- data output
6	ST	I	Chip shutdown. High level shuts down the chip; low level enables the chip
7	NC	--	No- connection, leave floating
8	XI	I/O	connect external crystal

2、Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	V_{DD}		-0.3	5.5	V
Interface pin voltage	V_{IN}		-0.3	V_{DD} + 0.3	V
Junction temperature	T_J		-40	125	℃
Storage temperature	T_{STG}		-50	150	℃
Soldering temperature	T_{SDR}	Duration ≤30 s		255	℃
ESD rating		Human- Body Model (HBM)	-2	2	kV
Latch- up current		@85 ℃	-100	100	mA

3、Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Symbol	Condition	Min		Max	Unit
Operating supply voltage	V_{DD}	-40℃~+85℃	2.1		5.5	V
Operating ambient temperature	T_{OP}		-40		85	℃
Supply- voltage slew rate	V_{SL}		1			mV/us

4、Electrical Characteristics

Table 4 Receiver Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Frequency range	F_{RF}	Achieved by selecting different crystals	300		490	MHz
Data rate	DR		1		5	kbps
Sensitivity	S	F_{RF} = 315 MHz, DR = 3 kbps, BER = 0.1%		-112		dBm
	S	F_{RF} = 433.92 MHz, DR = 3 kbps, BER = 0.1%		-113		dBm
Operating current	I_{DD}	F_{RF} = 315 MHz		5.0		mA
	I_{DD}	F_{RF} = 433.92 MHz		5.2		mA
Shutdown current	I_{SHUT}	SHUT SET		0.3		uA
Receiver bandwidth	BW	F_{RF} = 315 MHz		370		kHz
	BW	F_{RF} = 433.92 MHz		500		kHz
Receiver start- up time	T	ST falling edge to valid data output (CTH & AGC with 470 nF external capacitor)		4.0		ms
Saturated input level	P_{LVL}			-20		dBm
Input 3rd- order intercept point	IIP3	Two-tone test with 1 MHz & 2 MHz offset, maximum system gain setting		-29		dBm
Blocking immunity	BI	±1 MHz continuous-wave interference		28		dB
		±2 MHz continuous-wave interference		40		dB
		±10 MHz continuous-wave interference		59		dB
Co- channel rejection	CCR			-12		dB

5、Functional Description

5.1 Block Diagram

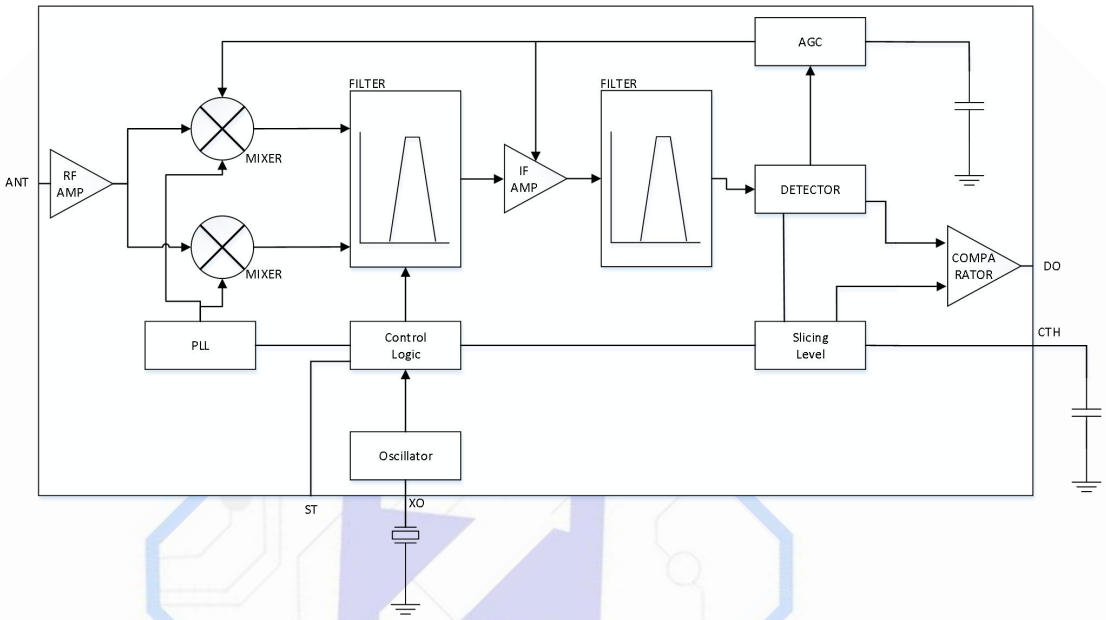

Figure 2 VI523R Internal Circuit Block Diagram

VI523R is a mixed-signal integrated receiver chip. It adopts a low-IF receiver architecture consisting of LNA + Mixer + IF Filter + Limiter + PLL. Stable data reception can be realized with only a small number of external components.

5.2 Crystal Frequency and RF Operating Frequency

VI523R implements a single-ended crystal oscillator circuit; load capacitance required for crystal oscillation is integrated inside the chip. It is recommended to use crystals with ±20 ppm frequency accuracy, equivalent series resistance less than 60 Ω, and 15 pF load capacitance. Please evaluate parasitic-capacitance differences for different crystal packages to avoid receiver-performance degradation caused by excessive crystal-frequency deviation.

VI523R works at any frequency point within the 300-490 MHz license-free band. The RF operating frequency is changed by selecting a corresponding crystal.

For 433.92 MHz RF operation: crystal frequency range 13.51783 MHz ~ 13.52127 MHz

For 315 MHz RF operation: crystal frequency range 9.8131 MHz ~ 9.81563 MHz

5.3 Receiver Intermediate- Frequency Bandwidth

When VI523R runs at 433.92 MHz, its IF bandwidth is 500 kHz. The IF bandwidth scales proportionally with the RF operating frequency determined by the crystal. Example: at 315 MHz, the IF bandwidth becomes 400 kHz.

5.4 Notes on CTH Component Selection

The CTH pin of VI523R must be fitted with an external data- filter capacitor. The CTH capacitance strongly affects start- up time and anti- interference performance.

For systems with severe power- supply or battery noise (e.g. AC- DC- powered systems or motor- equipped products): select larger capacitance (1 µF ~ 4.7 µF) to improve anti- interference capability, at the cost of longer chip start- up time.

For fast start- up requirements: select smaller capacitance (330 nF ~ 470 nF), which trades anti- interference performance for shorter start- up latency.

Choose the CTH capacitor value carefully according to system requirements.

6、Typical Application Circuit

6.1 Typical Schematic

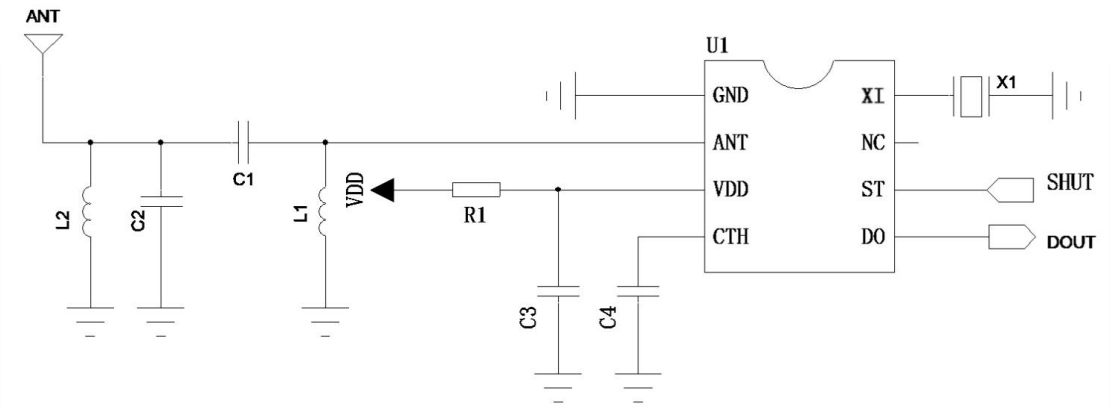

Figure 3 VI523R Typical Application Circuit

6.2 Typical Circuit BOM

Table 5 Reference BOM

Reference	Description	matched for λ/4 antenna		Unit	Supplier
		315MHz	433.92MHz		
X1	Crystal, ±20 ppm	9.8131 /9.81563	13.51783 /13.52127	MHz	
L1	Matching-network multilayer inductor, ±10 %	68	27	nH	
L2	Matching-network multilayer inductor, ±10 %	47	39	nH	
C1	Matching-network NP0 capacitor, ±0.25 pF, 50 V	3	3	pF	-
C2	Matching-network NP0 capacitor, ±0.25 pF, 50 V	4.7	3	pF	-
C3	Power-supply-filter X7R capacitor, ±20 %, 25 V	1		uF	-
C4	Data-filter X7R capacitor, ±20 %, 25 V	4.7	1	uF	
R1	Power-supply-filter resistor, ±5 %	47		Ω	-

7、Package

VI523R uses SOP8 package.

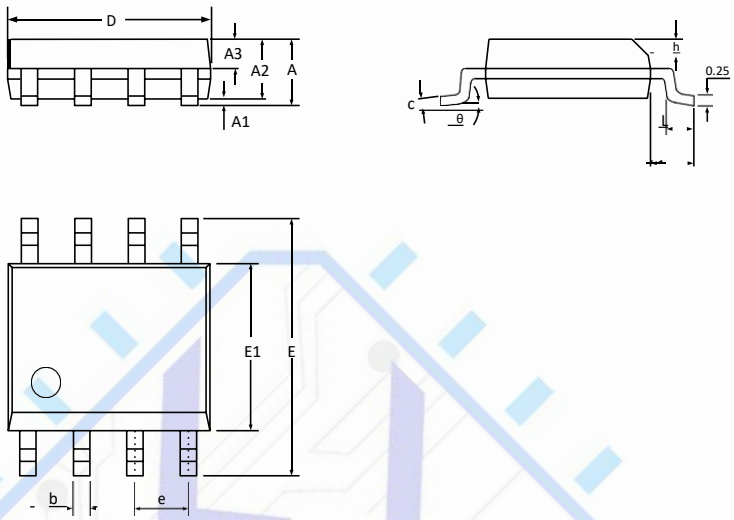

Figure 4 SOP8 Package

Table 6 SOP8 Package

Symbol	Dimensions (Unit: mm)		
	Min	Typ	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 BSC		
θ	0	-	8°